

an MOS transistor formed in a first area of the well which is isolated by the element  
isolation areas; and

a first conductivity type low resistance area provided at a base portion of the well area  
and having a resistive value lower than that of the well area.

#### REMARKS

Favorable reconsideration of this application as presently amended and in light of the  
following remarks is respectfully requested.

Claims 1-19 are presently active in this case; Claim 7 having been amended by way of  
the present Amendment.

In the outstanding Official Action, Claims 1-4, 7-10 and 13-16 were rejected under 35 USC  
§102(b) as being anticipated by Stolmeijer et al (U.S. 5,742,090); and Claims 5, 6, 11, 12, and  
17-19 were rejected under 35 USC §103(a) as being unpatentable over Stolmeijer.

In light of the several grounds for rejection, and in order to assure uniform claim  
interpretation, Claim 7 has been amended to state the same language as Claims 1 and 13 in  
regard to the recitation of "a first conductivity type low resistance area." Clearly no new  
matter has been added by this change to Claim 7.

Briefly recapitulating, a feature of claims 1, 7 and 13 is that the base portion of the  
well area has a low resistance area having a lower resistance than the well area. Similarly,  
Claim 16 recites that the base portion of the first well area has a low resistance area having  
lower a resistance than the first well area.

This feature of the claimed invention recited in the context of the variable capacitance  
of Claim 1, for example, has significance in that the resistance of the well can be maintained  
low even if the spaces between the wires are widened to reduce the capacity of wiring

connected to the electrodes of the condenser by the providing a low resistance area in the base portion of the well area. Accordingly, the structure defined in Claim 1 offers an advantage in that noise can be reduced.

Further, in the case of Claims 7 and 13, for example, where a MOSFET is formed in the well, the parasitic resistance of the well can be reduced by providing a low resistance area in the base portion of the well area. This offers advantages in that the power loss can be reduced and a high gain amplifier can be formed with the MOSFET.

Furthermore, in the case of a semiconductor device recited in Claim 16, in which an analog circuit and a digital circuit are merged, the claimed provision of a low resistance area in the base portion of the first well area offers an advantage in that a reduction in the gain of the analog circuit can be prevented.

Turning now to the applied Stolmeijer et al. patent, FIG. 5 of Stolmeijer et al. shows a CMOS device in which a P-well 130 and an N-well 230 are formed in the surface region of the substrate 10. In the surface regions of the P-well 130 and the N-well 230, active devices 100, 200 are formed as CMOS devices. The outstanding Office Action takes the position that the region 120 in P-well 130 and the region 220 in N-well 230 are low resistance areas corresponding to the claimed low resistance feature recited in Claims 1, 7, 13 and 16. However, the regions denoted by reference numerals 120 and 220 are field regions, as stated in column 3, lines 9-12, and column 3, lines 24-29 of the Stolmeijer et al. patent. Moreover, the field region 120 is nothing but the P-well 130 itself, and the field region 220 is nothing but the N-well 230 itself. In other words, the resistance of the field region 120 is equal to that of the P-well 130, and the resistance of the field region 220 is equal to that of the N-well 230. In contrast, pending Claims 1, 76, 13 and 16 state that the low resistance area has a resistive value lower than that of the well area. Therefore, it is respectfully submitted that the

Stolmeijer et al. patent fails to disclose structure corresponding to the "low resistance area" claimed in claims 1, 7, 13 and 16.

Accordingly, it is respectfully submitted that Claims 1, 7, 13 and 16, as well as claims depending therefrom, are not anticipated by Stolmeijer et al and that the outstanding grounds for rejection based on the Stolmeijer et al are traversed.

Consequently, in view of the present amendment and in light of the above comments, the pending claims are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.



Gregory J. Maier  
Attorney of Record  
Registration No. 25,599  
Eckhard H. Kuesters  
Attorney of Record  
Registration No. 28,870



22850

Tel.: (703) 413-3000

Fax: (703) 413-2220

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IN THE CLAIMS

Please amend Claim 7 as follows:

7. (Amended) A semiconductor device comprising:
  - a semiconductor substrate;
  - a first conductivity type well area formed in a surface area of the semiconductor substrate;
  - a plurality of element isolation areas formed in the well area;
  - an MOS transistor formed in a first area of the well which is isolated by the element isolation areas; and
  - a first conductivity type low resistance area provided at a base portion of the well area and having a resistive value lower than that of the well area.